AMENDMENTS TO THE DRAWINGS:

The attached eight (8) sheets of drawings include changes to Figs. 1-17. These sheets, which include Figs. 1-17, replace the original five (5) sheets of drawings, which included Figs. 1-17. See Paper # 5

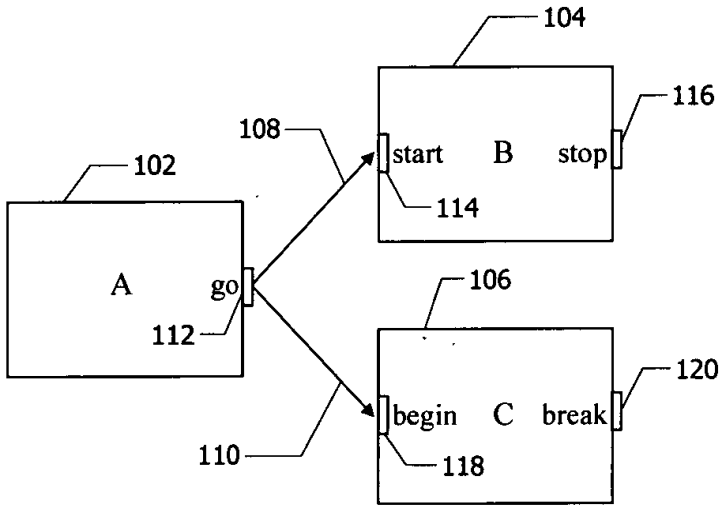

Fig. 1

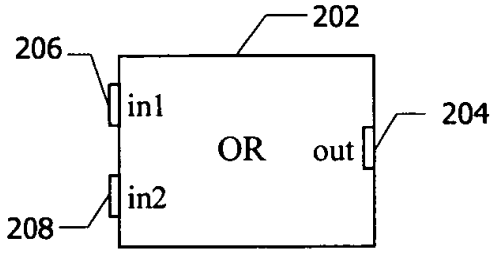

Fig. 2

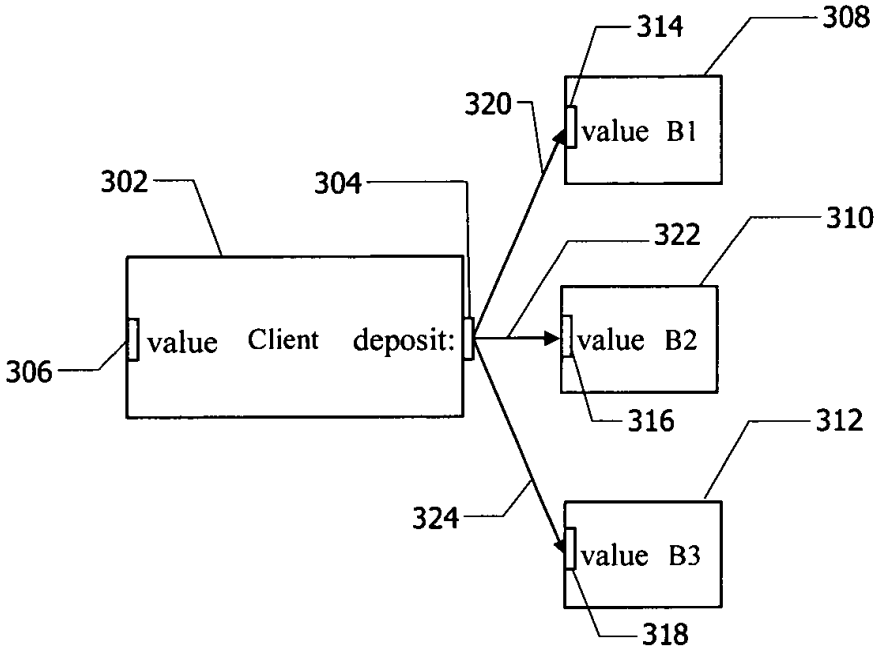

Fig. 3

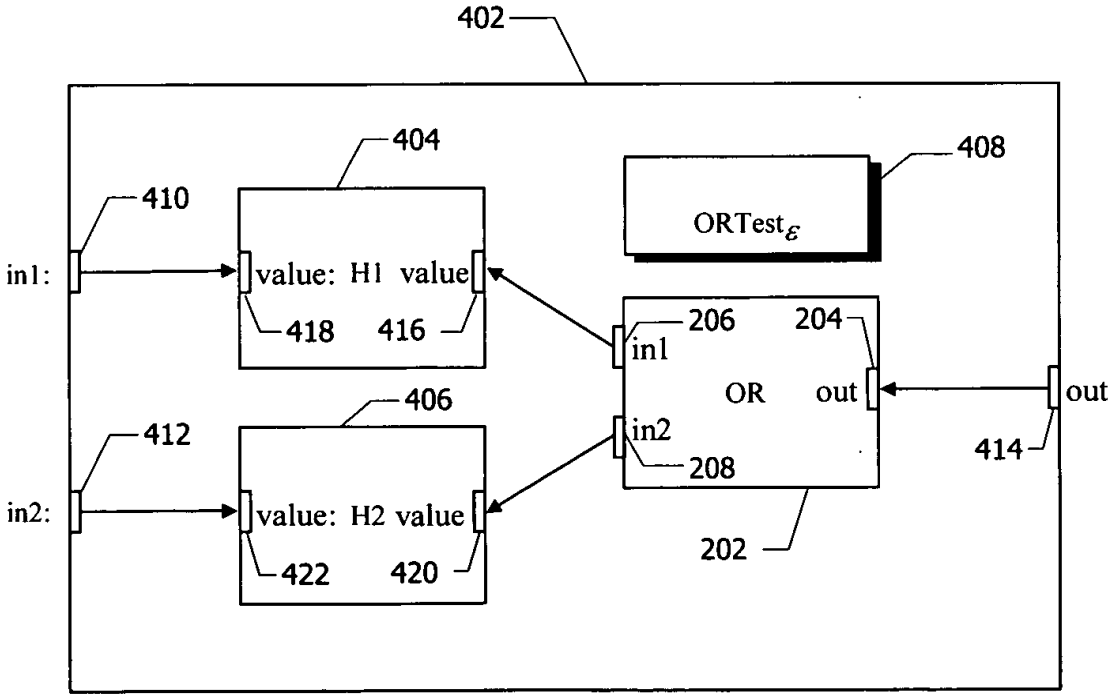

Fig. 4

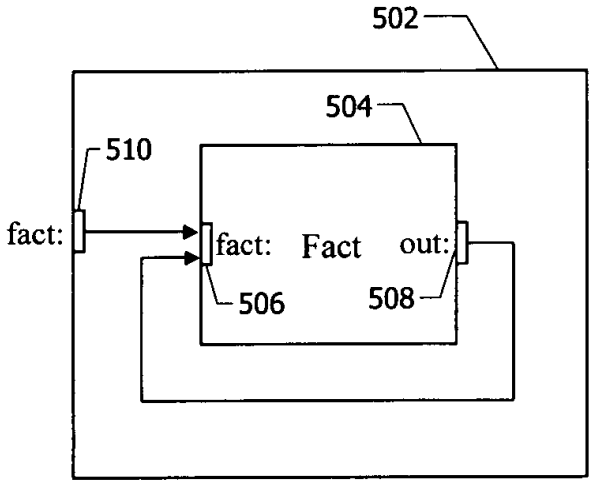

Fig. 5

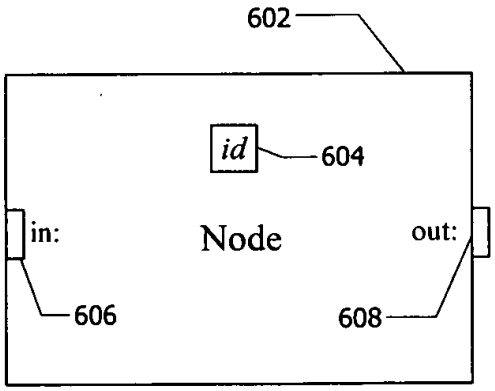

Fig. 6

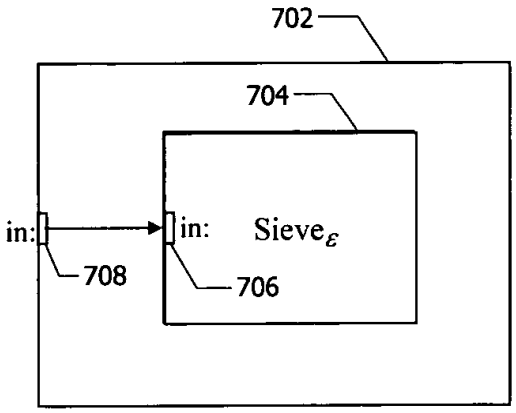

Fig. 7

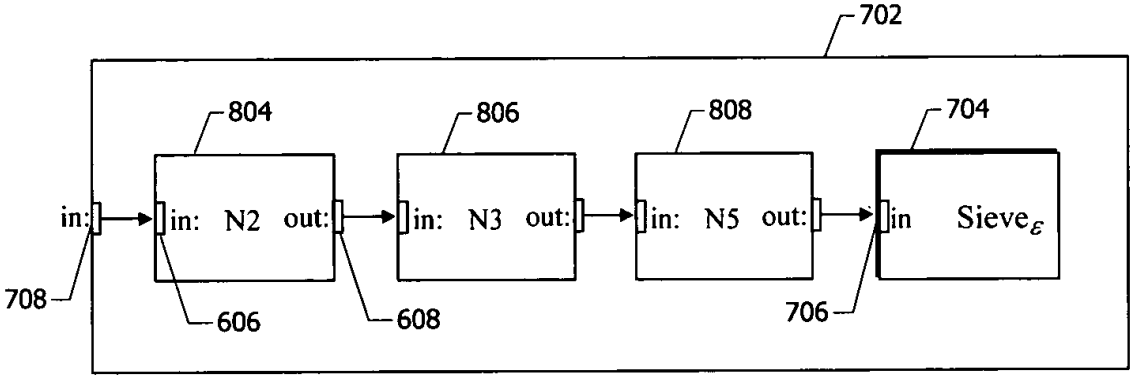

Fig. 8

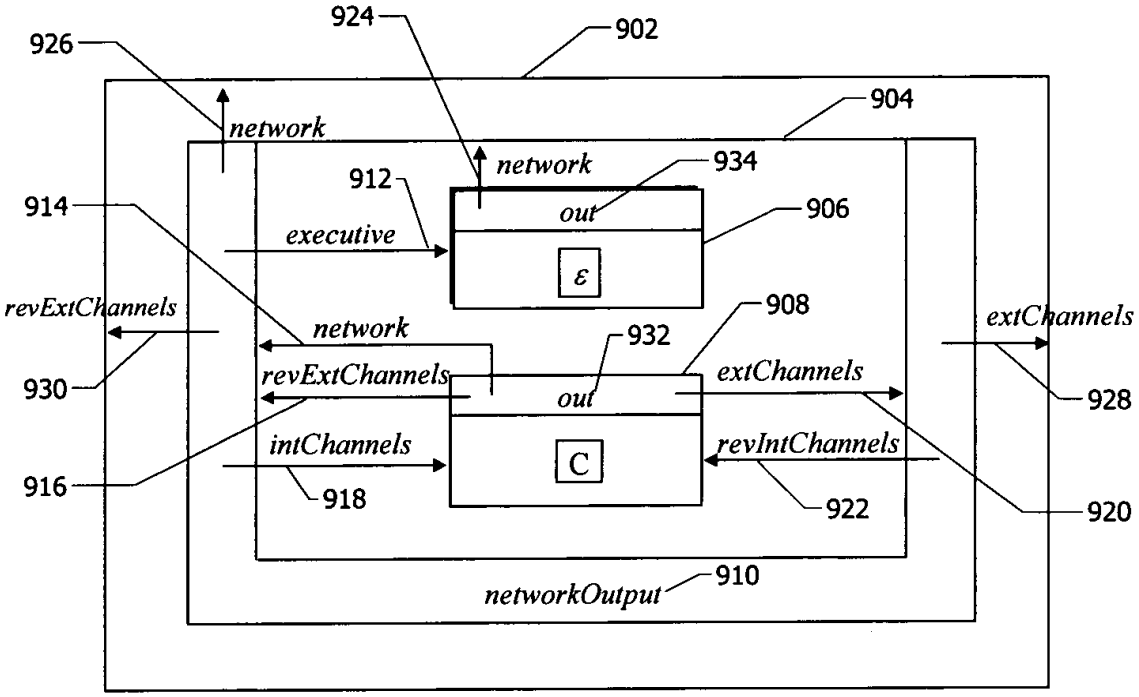

Fig. 9

```
Connecton
    Node
    And
    Or
    ...
    ConnectonExecutive
        Nand
        ORTest
        Sieve
        ...
```

Fig. 10

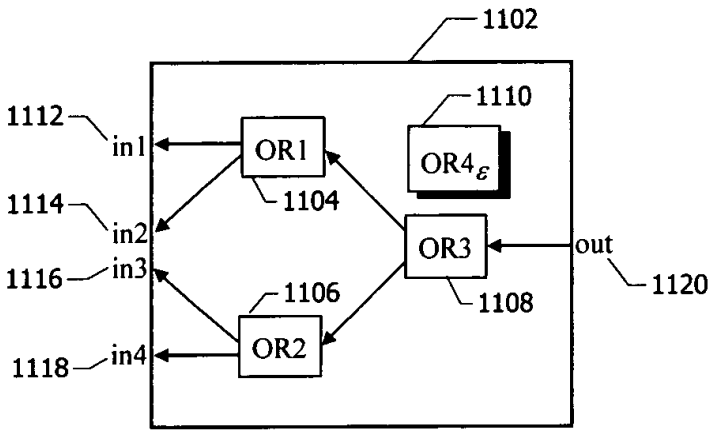

Fig. 11

```
connectonStructure
    |str|
    str := super connectonStructure.
    str addConnecton: #OR1 class: OR.
    str addConnecton: #OR2 class: OR.
    str addConnecton: #OR3 class: OR.
    str link: Network gate: #out to: #OR3 gate: #out.
    str link: #OR3 gate: #in1 to: #OR1 gate: #out.
    str link: #OR3 gate: #in2 to: #OR2 gate: #out.
    str link: #OR1 gate: #in1 to: Network gate: #in1.
    str link: #OR1 gate: #in2 to: Network gate: #in2.
    str link: #OR2 gate: #in1 to: Network gate: #in3.
    str link: #OR2 gate: #in2 to: Network gate: #in4.
```

Fig. 12

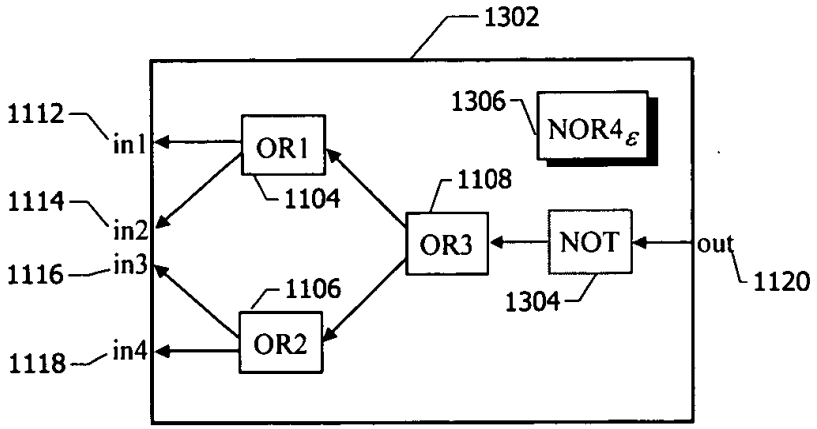

Fig. 13

```
connectonStructure
    |str|
    str := super connectonStructure.                    "Obtain the parent class structure"
    str addConnecton: #NOT class: NOT.                  "Add a not gate"
    str unlink: Network gate: #out from: #OR3 gate: #out.   "Unlink OR3 gate"
    str link: Network gate: #out from: #NOT gate: #out.     "Link the network output to the NOT gate output"
    str link: #NOT gate: #in from: #OR3 gate: #out.     "Link NOT to OR3 gate"
```

Fig. 14

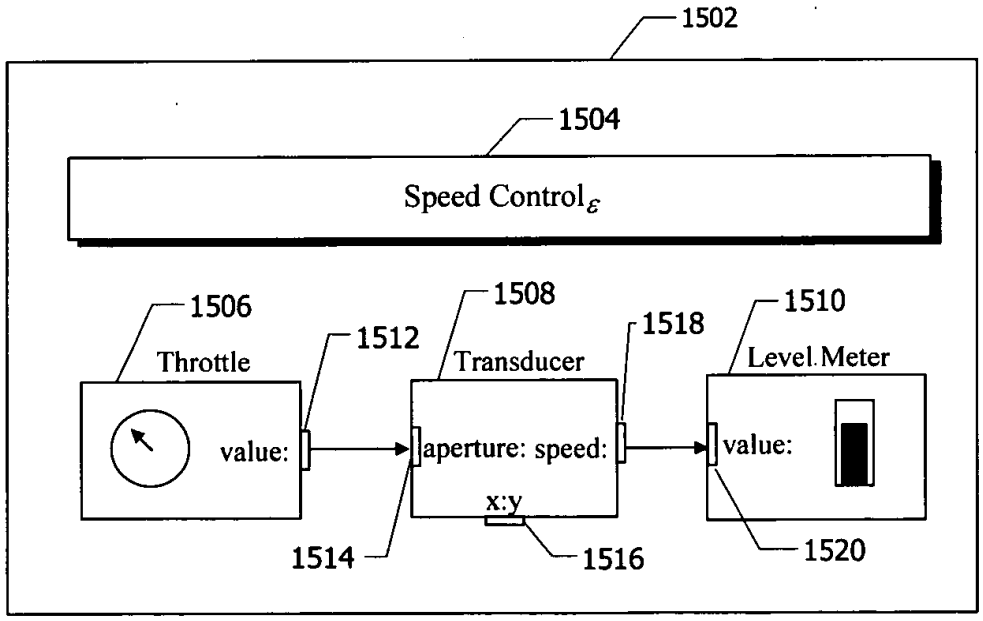

Fig. 15

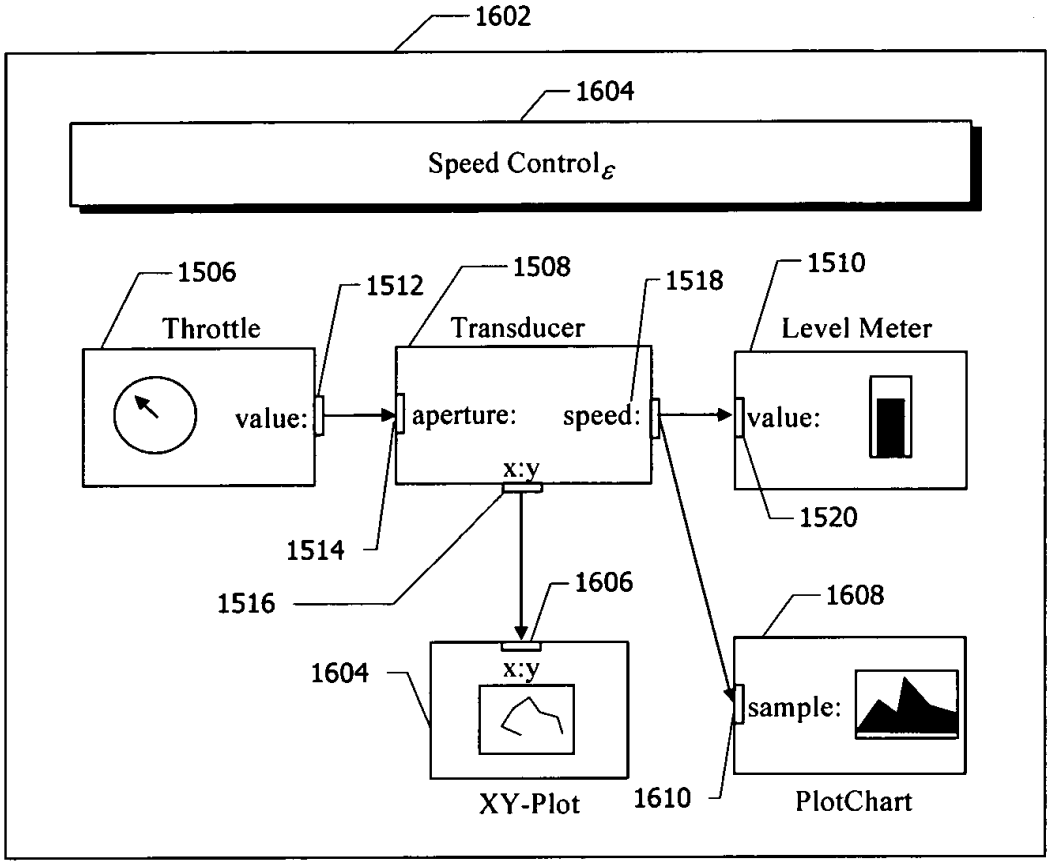

Fig. 16

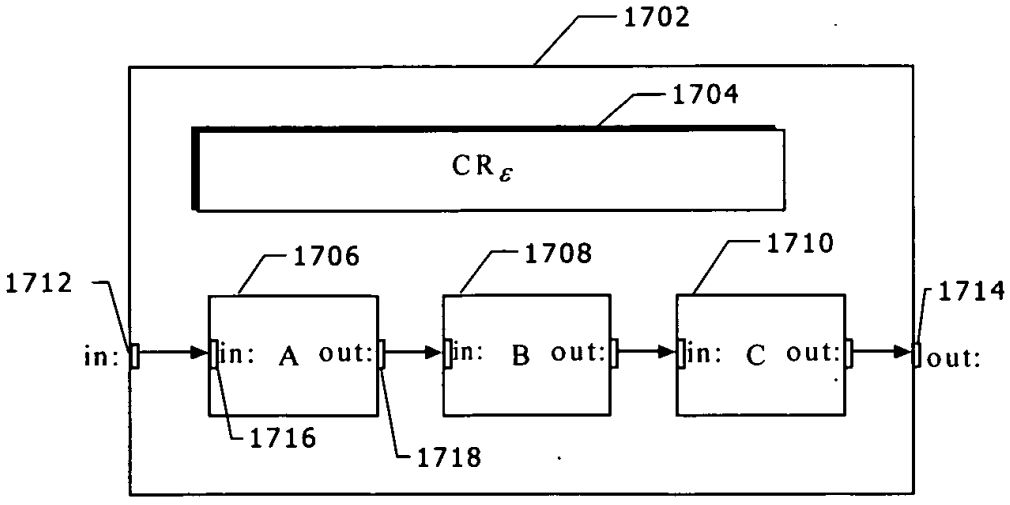

Fig. 17